-

INITIAL INFORMATION DATA SHEET

APPLICATION INFORMATION

Application Type::

Regular

Subject Matter::

Utility

Title::

Method and System for Flexible

Nesting JTAG Tap Controllers for

FPGA-Based System-On-Chip (SoC)

Docket Number::

X-1069 US

Request for Early Pub?::

No

Request for Non-Pub?::

Yes

Total Drawing Sheets::

Eleven

Small Entity?::

No

Petition included?::

No

INVENTOR INFORMATION

Inventor Authority Type::

Inventor

Primary Citizenship Ctry::

US

Status::

Full Capacity

Given Name::

David P.

Family Name::

Schultz

Street::

1762 Mirassou Place

City::

San Jose

State or Province::

CA

Postal or Zip Code::

95124

CORRESPONDENCE INFORMATION

Correspondence Customer Number::

24309

REPRESENTATIVE INFORMATION

Representative Customer Number::

24309

ASSIGNEE INFORMATION

Assignee Name:: Xilinx, Inc.

Street:: 2100 Logic Drive

City:: San Jose

State or Province:: California

Postal or Zip Code:: 95124